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Question Paper Code : 81230

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2025.

Third Semester

Electronics and Communication Engineering

EC 3352 – DIGITAL SYSTEMS DESIGN

(Common to Electronics Engineering (VLSI Design and Technology)/Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. State the DeMorgan's law.
2. List the advantages and disadvantages of Karnaugh map.
3. Write the logic equation for 4-bit magnitude comparator.
4. Draw the logic diagram for full adder circuit.
5. What is master-slave flip-flop?
6. Define setup and hold time.
7. Differentiate between fundamental and pulse mode asynchronous sequential circuits.
8. List the differences between synchronous and asynchronous circuits.
9. What is fan-in and fan-out of a circuit?
10. Differentiate EPROM, EEPROM and EAPROM.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Convert the Boolean function $F = AB + A'C + B'C'$ into canonical SOP and POS forms. (6)

- (ii) Simplify a 4-variable Boolean function.

$F = m(1, 5, 6, 11, 12, 13, 14) + d(4, 15)$ using Karnaugh map with don't care conditions and draw the logic diagram. (7)

Or

- (b) Apply tabulation method to simplify the function $F(A, B, C, D) = \Sigma(0, 1, 2, 5, 6, 7, 8, 9)$ and draw the logic diagram using NAND gates only.

12. (a) (i) Design a 4-bit binary to Gray code converter using logic gates. (10)

- (ii) Design a BCD adder circuit. (3)

Or

- (b) (i) Explain the operation of 4-bit carry look-ahead adder logic. (6)

- (ii) Design a 4-bit parity generator and checker circuit. (7)

13. (a) Explain the working of a universal shift register with operation modes.

Or

- (b) A sequential circuit with 2D FFs A and B and input X and output Y is specified by the following next state and output equations.

$$A(t+1) = AX + BX; B(t+1) = A'X; Y = (A + B)X'.$$

- (i) Draw the logic diagram of the circuit.

- (ii) Derive the state table and

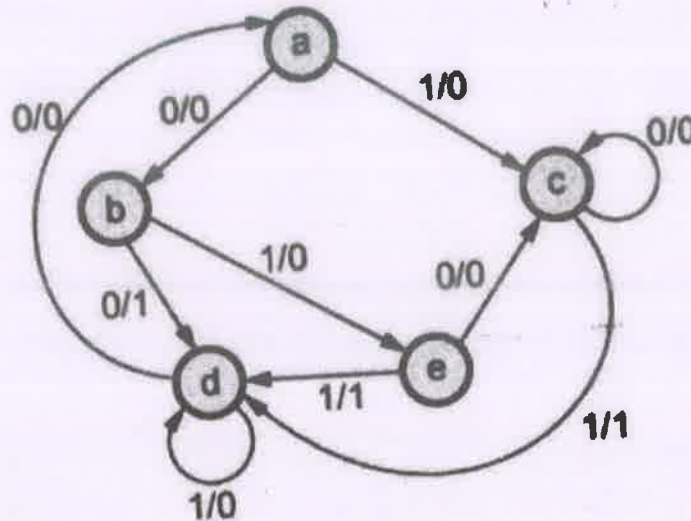
- (iii) Derive the state diagram.

14. (a) Design a hazard-free circuit for a simple logic function

$$F(P, Q, R) = QR + PR$$

Or

- (b) Obtain the final state diagram by applying the state reduction technique to the following state diagram.



15. (a) (i) Explain the CMOS logic family with necessary diagram. (7)
 (ii) Compare RTL, TTL and ECL families using various parameters. (6)

Or

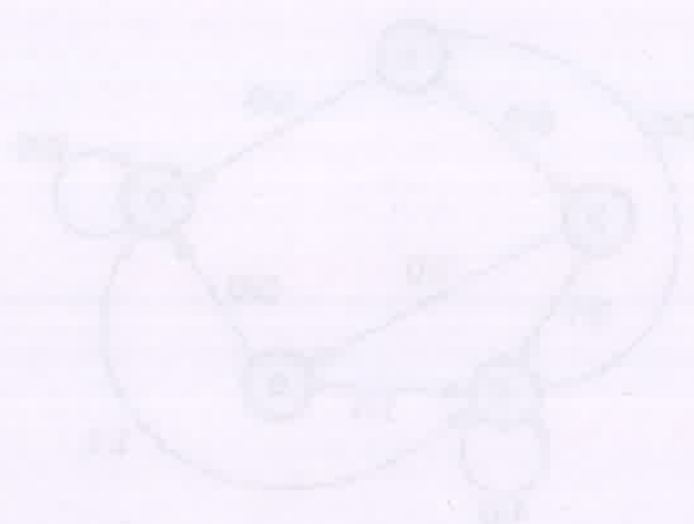
- (b) (i) Implement a 3-bit counter using a PROM. (7)
 (ii) Compare the features and applications of PROM, PLA, and PAL. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Design a 4-bit synchronous up-counter using T flip-flops.

Or

- (b) (i) Design and implement a BCD to 7-segment decoder using PAL. (10)
 (ii) Design a rolling display. (5)



1. Find the shortest path from node 1 to node 7.
2. Find the shortest path from node 2 to node 7.
3. Find the shortest path from node 3 to node 7.
4. Find the shortest path from node 4 to node 7.
5. Find the shortest path from node 5 to node 7.
6. Find the shortest path from node 6 to node 7.
7. Find the shortest path from node 7 to node 1.
8. Find the shortest path from node 7 to node 2.
9. Find the shortest path from node 7 to node 3.
10. Find the shortest path from node 7 to node 4.
11. Find the shortest path from node 7 to node 5.
12. Find the shortest path from node 7 to node 6.